Multi-Project Chip Activities in Korea
- IDEC Perspective -

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Abstract— This paper describes the current status of multi-project chip(MPC) services in Korea to promote full-custom and semi-custom IC design activities in universities. Although MPC foundry services for IC designs were started in a lesser scale more than 10 years ago, it is only recent that systematic and effective educations and MPC foundry services program called IDEC(IC design education center) was launched with the planned support of the government and three major semiconductor companies in Korea. In this paper, we introduce the activities of IDEC and other MPC foundry services currently being provided.

I. Introduction

Today's non-memory chip design is a basic value-added technology in the industries of communication, consumer, and vehicular electronics. Until recently, however, most of the Korean semiconductor industries have focused on the memory devices, while the non-memory IC and system design skills including CAD and library development have relatively fallen behind, thereby having poor competitiveness in the international market as a whole. Generally, the non-memory chip design requires highly experienced designers and it takes a long time to produce an expert. Moreover, designs of qualified chips which are competitive require not only circuit design techniques but also close co-working of various areas related to the chip designs, as indicated in Fig. 1. Recently, as the government have recognized the importance of the chip design technologies and highly experienced designers, a national policy has been established to make the Korean semiconductor and system industries competitive for the coming 21st century.

This paper briefly describes the current status of multi-project chip(MPC)[1] services in Korea, to promote full-custom and semi-custom IC design activities in universities. Educational programs and MPC foundry services for VLSI and system designs were started, for the first time, through the ISRC(Inter-University Semiconductor Research Center)[4] in 1991. Recently, with the assistance of the government and three major semiconductor companies in Korea, a systematic and effective mechanism called IDEC(IC Design Education Center) [2] [3] for education and MPC foundry service for VLSI and system designs was started in 1995.

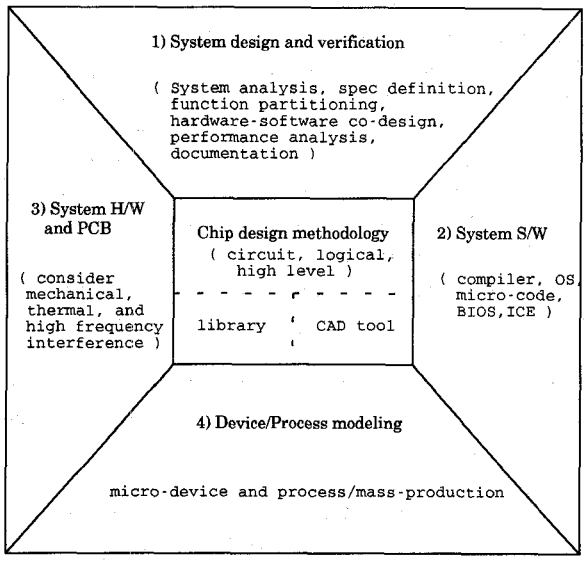

Fig. 1. Areas related to semiconductor chip design

Three nation-scale workshops were held during 1994-1995 where the selection process, support scale and strategy as well as the functions and characteristics of the organization, which will be responsible for the promotion of IC and system design activities in universities, were rather thoughly discussed among university professors, government officials and managers in semiconductor companies. After a lengthy and systematic procedure for selecting the host organization to perform the task, KAIST was cho-

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sen through the vote among universities, companies, and government in the final workshop in April, 1995 where 7 universities have competed.

The organization of this paper is as follows: we introduce the IDEC and its function in section II, and other MPC foundry services are briefly described in section III.

II. IDEC(IC Design Education Center)

IDEC was founded at KAIST (Korea Advanced Institute of Science and Technology) in 1995, with the support of MOTIE (Ministry of Trade, Industry, and Energy) and three major semiconductor companies (Hyundai Electronics, LG semicon and Samsung Electronics). The main objective of IDEC is to foster highly-qualified VLSI and system designers by providing a variety of lectures, textbooks, video materials to all domestic university students, as well as the MPC service. IDEC also aims to promote the VLSI design activities by establishing complementary exchange programs between universities and industries. Thereby the IDEC intends to balance the memory and non-memory business activities in the Korean semiconductor and system industries, and to encourage university graduates' inherent motivation, creative talent, cooperative spirit, and general knowledge.

The main functions of the IDEC is largely divided into four:

1. Providing IC design environment to universities through the support of CAD tools and computer equipments,
2. VLSI design education and training on the design methodology and how to use CAD tools, etc,
3. Development of textbooks and video materials for VLSI and systems design, and
4. MPC fabrication service (as an interface).

A. Support of CAD Tools and Computer Equipments

The IDEC provides the most needy domestic universities with CAD tools and WS/PC hardware equipments necessary for VLSI design education, by the assistance from the government and semiconductor companies. During the first year, a total of about 80 universities have applied to the IDEC for CAD tools and computing equipments, among which 38 universities were finally selected, as shown in Table I. The CAD tools distributed to the selected universities are shown in Table II. Xilinx FPGA tools are now being distributed to each universities. We plan to support 60 universities during the second year, 65 during the third year, and 70 universities during the fourth year, as summarized in Table III.

TABLE I
Working groups selected in the first year

Ajou	Anyang	Chonnam
Chonbuk (Dept. EE)	Cheju	Chungang
Chongju	Chungnam	Chungbuk
Dongguk	Hanyang (Seoul)	Hanyang (Ansan)
Inchon	KAIST	Kangnung
Kangwon	Konkuk	Kyungpook
Kyungsang	Kyunghee	Korea
Kongju	Kwangwoon	Kookmin
Kumoh	Pusan	Pusan tech.
POSTECH	Sogang	Sokung
Seoul	Seoul city	Sungkyunkwan
Yonsei (Dept. CE)	Yonsei (DEpt. EE)	Soongsil
Ulsan	Wonkwang	Yeungnam

TABLE II
CAD tool list supported to working groups in universities

Tool	# of working groups supported
Altera	41
Cadence	36
COMPASS	36
Hspice	38
Mentor	35
MyCAD	30
Synopsys	38
Xilinx	41(scheduled)

TABLE III
IDEC Plan for 4 years

Support	1st	2nd	3rd	4th
# of Working groups supported	41	60	65	70

B. VLSI Design Education and Training on CAD Tools

The IDEC offers a variety of educational lectures, seminars, and short-course mainly for university students and engineers in companies or institutes. The lectures are open about every two weeks, and covers the topics necessary for VLSI design, from basic CMOS analog/digital circuit designs to top-level system designs.

TABLE IV
LIST OF LECTURES HELD IN IDEC IN THE FIRST YEAR(1996)

Lecture
- Analog & Mixed Mode IC Design
- ASIC Design for Communication & Signal Processing
- Digital VLSI System Design
- ASIC Design using FPGA
- Design Methodology on System Level
- CMOS IC Design Basic Practice
- Analog IC Design
- VLSI Implementation of DSP Algorithms
- Basics of Digital VLSI Testing
- Analog/Digital Subsystem Design
- Video IC Design
- VHDL: Theory & Practice
- ASIC Design Using FPGA
- High Speed VLSI Interconnection & Packaging
- MOS Process & Device for IC Designer
- The Concept & Application of Emulation
- Verilog: Theory & Practice
- Low Voltage, Low Power IC Design Technology
- Semiconductor Memory Design
- HDTV ASIC Short Term Course
Tool Education
- COMPASS Tool
- MyCAD Tool
- Hspice Tool
- Mentor Tool
- Synopsys Tool
- Mentor Tool(GDT & Lsim)
- Xilinx Tool
- Top-Down ASIC/FPGA Design & Implementation for Mentor Tool
H/W Education
- System Administration of HP & SUN

Since KAIST is located in the center of Daeduk Science Town, its educational and research activities are shared with nearby universities and institutes. Most of the lectures are accompanied by experiments, so that the students can learn not only the theory but also the implementing method by using CAD tools. In addition, the CAD tool training educations are periodically carried out for VLSI design beginners. Table IV describes the title of lectures that were held so far in IDEC.

C. Development of Textbooks and Video Materials

One of the IDEC's activities is to make textbooks and video tapes regarding VLSI and systems design. The textbooks are being made for university education and industry training. For the effective and practical education, highly experienced lecturers are selected. The textbooks treat not only basic theories but also practical problems. Table V shows the list of textbooks to be published at the end of the first year(1996) or the beginning of 1997. Also, IDEC provides a variety of video tapes. The lectures are recorded on the video tapes and distributed to all universities according to their demands at a very competitive price. Therefore, the university students or engineers can take all lectures at home or office. During the first year, a total of 25 lectures have been recorded, and we are planning to provide more video tapes covering various topics.

TABLE V
LIST OF TEXTBOOKS TO BE PUBLISHED AT THE END OF 1ST YEAR

Semiconductor Device and Process for IC Design
Testing & Design for Testing
Design of DRAM
Basics and Applications of VHDL
ASIC Design using FPGA
Analog IC Filter Design
IC Design Verification: Simulation and Emulation
Introduction of CAD for Digital System Design
VLSI Design: Theory & Practice
VLSI System Interconnection Model and Analysis

D. MPC foundry interface

The final goal of the IDEC function is to foster competent designers who have the practical sense by measuring and analyzing the result of the fabricated chip. For this, the IDEC offers all graduate and undergraduate students an opportunity to implement their dedicated designs, and hence encourages their inherent motivation, creative talent, and general knowledge. As IDEC has no own fabrication facility, it only plays an interfacing role between the designers and companies. For the MPC foundry service, three major semiconductor companies provide various analog and digital fabrication processes, as summarized in Table VI. During the first year, a total of 173 designs were received as MPC candidates, among which 68 designs were selected based on the following criteria: originality, expectation of success and educational effect. Only a few of them are listed in Table VII. They are now

being fabricated and will be forwarded to each designers by the end of this year. We plan to gradually increase the total number of MPC service, roughly 150 chips in the second year, 200 in the third year, and 250 in the fourth year.

TABLE VI
IDEC MPC SERVICE IN 1996

Company	Process	Chip size (in mm)	Package
LG semiconductor	1-poly, 2-metal 0.8 μm CMOS	5 X 5	100 pin QFP
Hyundai electronics	1-poly, 2-metal 0.8 μm CMOS	5 X 5	100 pin QFP
	0.8 μm SOG	5 X 5	100 pin QFP
Samsung electronics	0.8 μm SOG	5.3 X 5.3 4 X 4	100 pin QFP

TABLE VII
LIST OF A FEW IDEC MPC DESIGNS IN 1996

VLC and multiplexing block of MPEG2
JPEG CODEC using modified Huffman code
A new digital filter without multiplier for real-time image processing
HMM edge detector
Dynamic weight warping ASIC for image recognition
Systolic array motion estimator
CSD filter for pre-processing of image signal
3D graphics display controller
ATM switch using neural network
Low power unlocked RISC processor
IS-95 PN code transmitter
51.84 Mbps CAP signal generator
Design of a built-in current sensor for loop testing
A VLSI implementation of new division algorithm based on lookahead of partial remainder
Video sync separator
Wavepipelined multiplier using CCPL
Adiabatic circuits and supply clock generator
Neural network chip for feature extraction
Fourth order sigma-delta modulator
Continuous time filter for medical application

III. OTHER MPC SERVICES

A. ISRC(Inter-University Semiconductor Research Center)

ISRC was established in the Seoul National University campus on July 12, 1985 as a government-funded organization, recognizing the importance of micro-electronics as the base technology of modern industry. The facilities in the ISRC are open to any university and industry affiliates for research, development, and education. The goals of the center are as follows:

1. to provide a central, common base for the university researches to perform the state-of-the-art research and development in the area of semiconductor process and design.
2. to educate undergraduate, graduate and continuing students from industry by exposing them to real-world problems
3. to perform joint research and development work between academia, research institutes, and industry.

ISRC began MPC services in 1991 to support designs of universities and mid/small-sized industries using its own 1.5 μm CMOS technology in which capacitor and double metal layers are provided. ISRC MPC service handles about 10 full-custom chips three times a year on the average, and turn-around time counted from the point of collecting design data to the point of returning fabricated chip takes about 4 months. Table VIII shows die sizes and package type available in ISRC.

TABLE VIII
ISRC DESIGN TECHNOLOGY FOR MPC

Technology	1.5 μm doule metal n-well CMOS with capacitor
Data format	GDSII
Die size	3 mm by 3 mm, 3mm by 4mm
Package	40 pin DIP
Pad frame	40 pin, 44 pin ISRC regulation.

To support design verification and measurement, ISRC provides educations on measurement equipments such as probe station, probe card, IMS tester, parameter analyzer and digital oscilloscope.

B. LG semicon design contest

Since 1995, LG semicon began to offer IC design contest to university students with some attractions as prizes. Through a careful evaluation of design proposals submitted by universities, designs to be fabricated are selected. The evaluation is performed by leading authorities

in academia and related areas on the basis of creativity, effectiveness and practicality. For the selected designs, LG semicon provides fabrication and gives encouragement awards to outstanding designers. VLSI circuits to be submitted to the IC design contest should be designed with full-custom method using 0.8 μm CMOS technology design rule provided by the company. Table IX describes the technology briefly, and Table X lists a few design rule parameters used in the full-custom layout.

TABLE IX
PROCESS CHARACTERISTICS OF LG SEMICON FOR MPC

0.8 μm CMOS technology (single poly, double metal)
9 - 12 Ohm.cm substrate
Twin-tub, self-aligned well structure
LOCUS isolation
gate oxide 155 A
polycide gate structure with CVD WSi2
SOG process for inter-metal planarization
No die coating process

TABLE X
LG SEMICON DESIGN PARAMETERS FOR MPC

Minimum gate length	0.8 μm
Minimum contact hole size	0.8 μm X 0.8 μm
Minimum metal line width	1.4 μm
Minimum active width	1.4 μm
Minimum field width	1.0 μm

The selected designs are packaged with 100 pin QFP, and maximum chip size supported is 5 X 5 cm^2 without scribe lane. Table XI shows the titles of the designs which took the prize in 1995.

TABLE XI
DESIGNS THAT TOOK THE PRIZE AT THE IC DESIGN CONTEST OF LG SEMICON IN 1995

Pipelined(63,51) DEC BCH CODEC using algorithmic computation
Design of Low noise RF frequency synthesis for digital mobile communication
High speed D/A converter for digital communication
Oversampling A/D converter using parameterizable quantizer
LPF for audible frequency based on CMOS switched capacitor
Design of wave-pipelined multiplier
900 MHz PLL design for hand-held phone
VLSI design of lossless data compressor having effective structure using the locality of matching length
Current mode 7 bit 20 Mhz pipelined CMOS ADC
3V 10 bit DAC
Design of high speed current mode ADC

IV. SUMMARY AND CONCLUSIONS

The IDEC is a government-initiated nonprofit organization to foster competent VLSI designers through the support of educational activities in universities related with VLSI design such as providing lectures, textbook and video production, MPC services, etc.

In the first year(1996), 41 working groups in 38 universities were provided with some number of workstations, PC's and CAD softwares as an initial environment. At the end of each year, the performance of each working group is evaluated according to various criteria including the number and quality of MPC-fabricated chips, participation in the educational lectures, and so on, and the result will be used to decide the level of support to each working group in the next year. IDEC is the most systematic and full-fledged operation to support and promote IC design activities in universities in Korea, and is expected to significantly contribute to the education of engineers and leveling-up of the systems and IC design expertise as a whole, along with other MPC foundry services in Korea mentioned.

REFERENCES

[1] C. Mead and L. Conway, *Introduction to VLSI Systems*, Addison Wesley, 1980

[2] IDEC Guide Brochure - 1996

[3] IDEC Web Home Page, *http://idec.kasit.ac.kr*

[4] ISRC Web Home Page, *http://chips.snu.ac.kr*